

CT30A2001
Tietoliikennetekniikan perusteet

Data and Computer Communications

Eighth Edition

by William Stallings

**Chapter 6 – Digital Data Communications
Techniques**

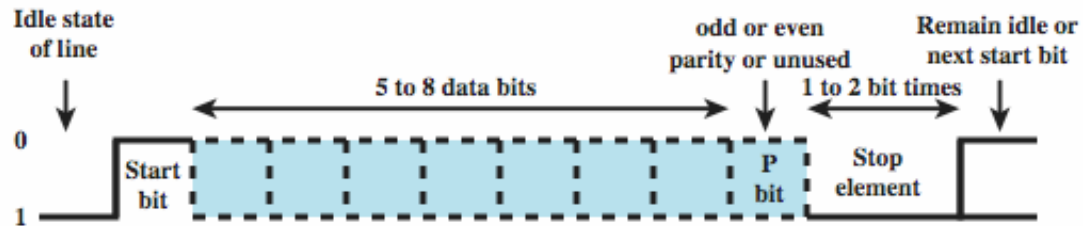
Lecture slides by Lawrie Brown

Partly modified/translated by J. Porras

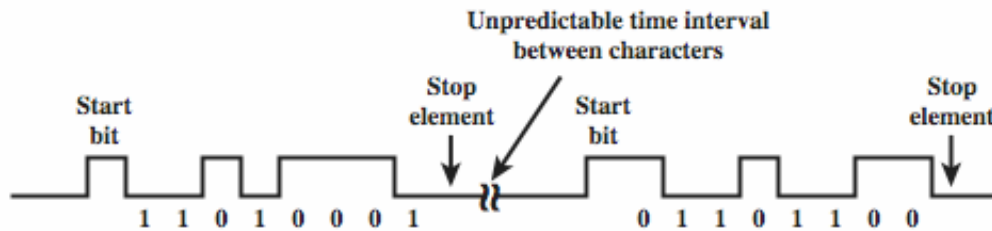
Asynchronous and Synchronous Transmission

- timing problems require a mechanism to synchronize the transmitter and receiver
 - receiver samples stream at bit intervals
 - if clocks not aligned and drifting will sample at wrong time after sufficient bits are sent
- two solutions to synchronizing clocks
 - asynchronous transmission
 - synchronous transmission

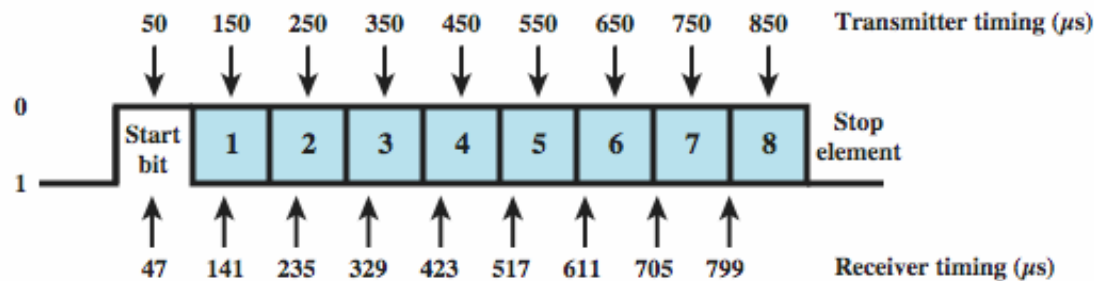
Asynchronous Transmission



(a) Character format



(b) 8-bit asynchronous character stream



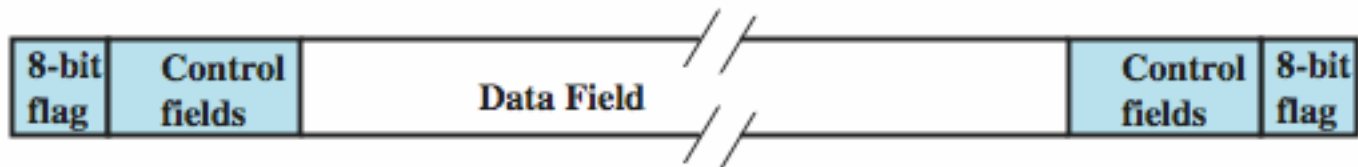
(c) Effect of timing error

Asynchronous - Behavior

- simple
- cheap
- overhead of 2 or 3 bits per char (~20%)
- good for data with large gaps (keyboard)

Synchronous Transmission

- block of data transmitted sent as a frame
- clocks must be synchronized
 - can use separate clock line
 - or embed clock signal in data
- need to indicate start and end of block
 - use preamble and postamble
- more efficient (lower overhead) than async



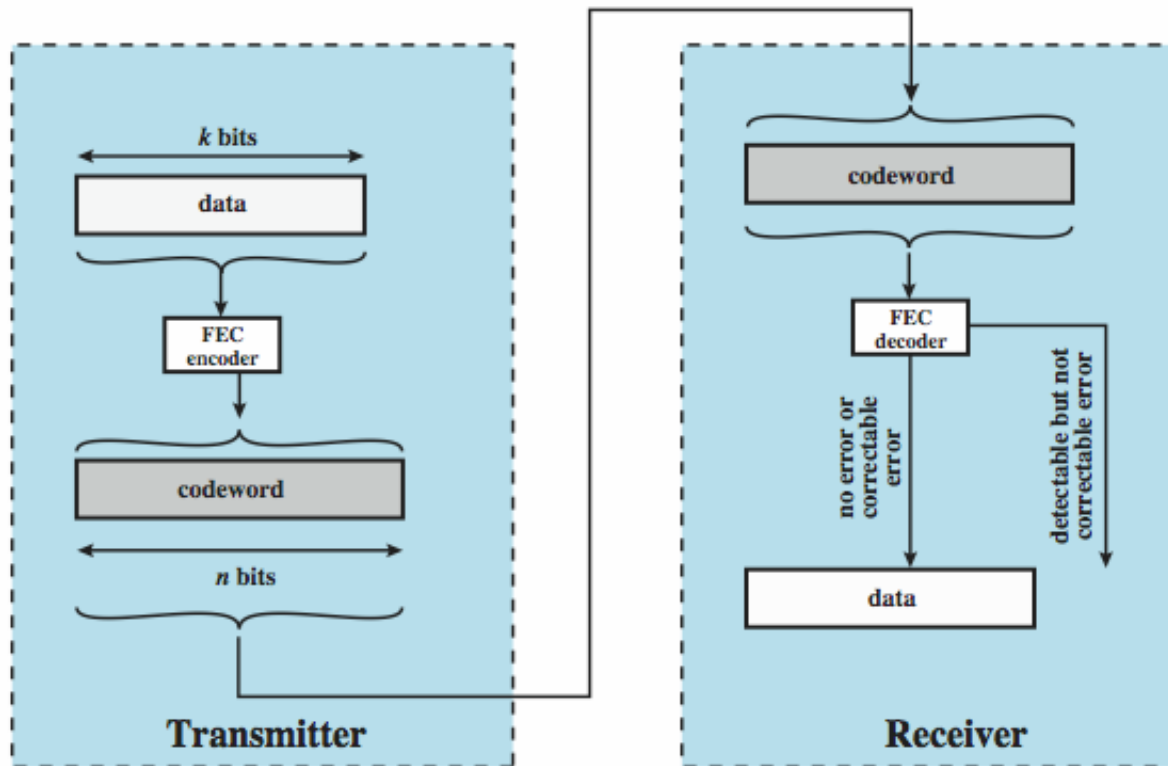
Types of Error

- an error occurs when a bit is altered between transmission and reception
- single bit errors
 - only one bit altered
 - caused by white noise
- burst errors
 - contiguous sequence of B bits in which first last and any number of intermediate bits in error
 - caused by impulse noise or by fading in wireless
 - effect greater at higher data rates

Virheen havainnointi

- will have errors
- detect using error-detecting code
- added by transmitter
- recalculated and checked by receiver
- still chance of undetected error
- parity
 - parity bit set so character has even (even parity) or odd (odd parity) number of ones
 - even number of bit errors goes undetected

Error Detection Process



Cyclic Redundancy Check

- one of most common and powerful checks
- for block of k bits transmitter generates an n bit frame check sequence (FCS)
- transmits $k+n$ bits which is exactly divisible by some number
- receiver divides frame by that number
 - if no remainder, assume no error
 - for math, see Stallings chapter 6

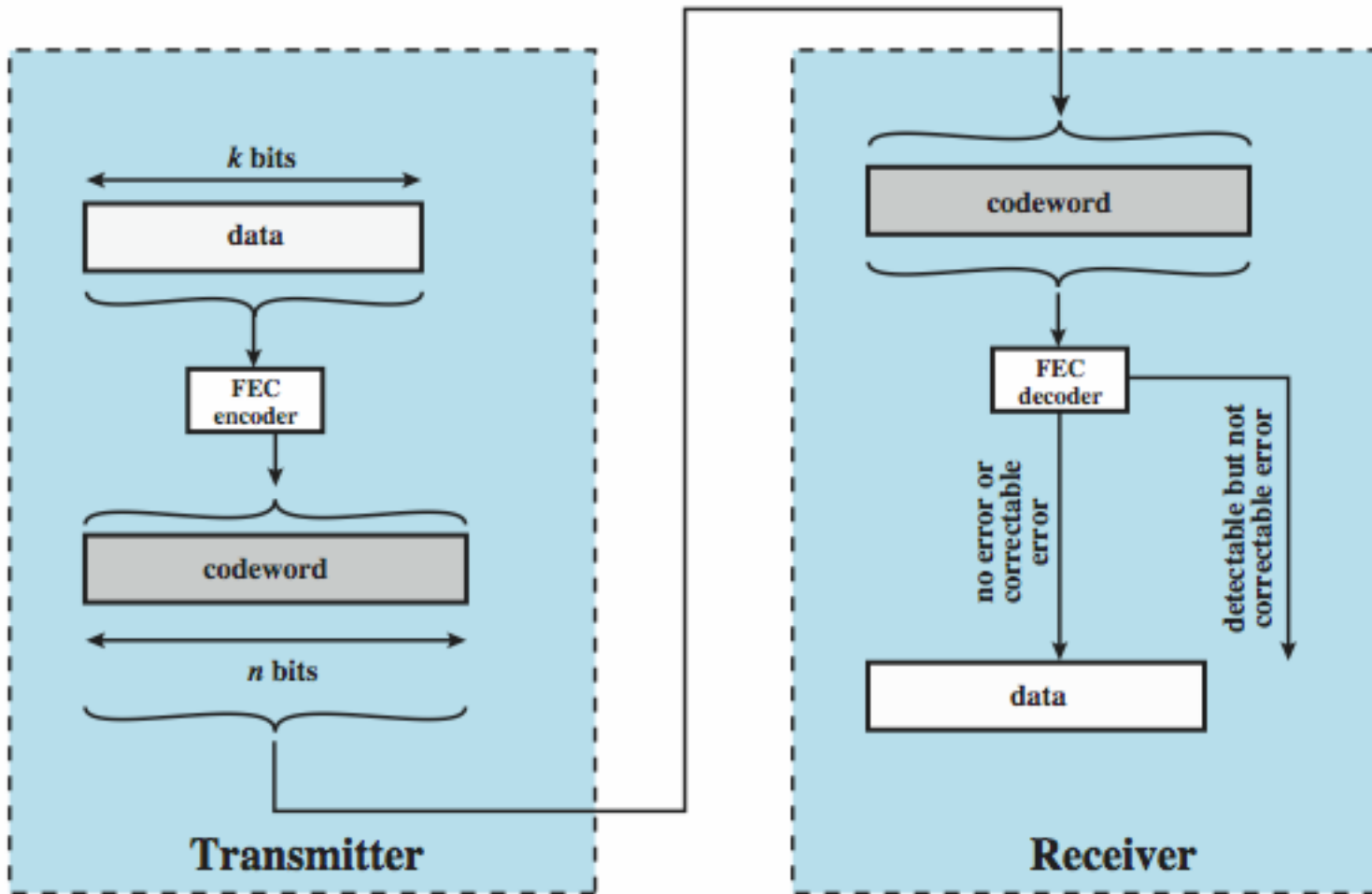
Polynomit

- Toinen tapa esittää CRC
 - $D(X) = X^5 + X^4 + X + 1$ (=110011)
- Tyypillisiä CRC funktioita
 - CRC-12 = $X^{12} + X^{11} + X^3 + X^2 + X + 1$
 - CRC-16 = $X^{16} + X^{16} + X^2 + 1$
 - CRC-CCITT = $X^{16} + X^{12} + X^5 + 1$

Virheen korjaus

- correction of detected errors usually requires data block to be retransmitted
- not appropriate for wireless applications
 - bit error rate is high causing lots of retransmissions
 - when propagation delay long (satellite) compared with frame transmission time, resulting in retransmission of frame in error plus many subsequent frames
- instead need to correct errors on basis of bits received
- error correction provides this

Error Correction Process



How Error Correction Works

- adds redundancy to transmitted message
- can deduce original despite some errors
- eg. block error correction code
 - map k bit input onto an n bit codeword
 - each distinctly different
 - if get error assume codeword sent was closest to that received
- for math, see Stallings chapter 6
- means have reduced effective data rate